Available online at www.ijiere.com
International Journal of Innovative and Emerging Research in Engineering
e-ISSN: 2394 - 3343 p-ISSN: 2394 - 5494

Simulation Of Three Phase Multilevel Inverter With Reduced Number Of Switches

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ABSTRACT:
Multilevel inverter having wide range of application just because of its flexibity, easier control, less cost and less area. Multilevel inverter can be used in small as well as medium and large power application. In MLI output voltage can be obtain pure with help of appropriate control strategy.THD of output voltage of MLI is quite less. Despite of all advantages MLI having issued with higher number of power electronics components. As number of switches increases voltage drop related to switch increases. Moreover, switching loss as well as overall converter loss increases. Main focus of study is to decrese power semiconductor switches for particular levels.A multilevel dc link using fixed dc voltage supply and cascaded half-bridge is connected in such a way that the new inverter outputs the required output voltage levels. For the purpose of increasing the number of voltage levels with fewer number of power electronic components, the structure of the new topology has been developed.

Keywords: Multilevel Voltage Source Inverter, Symmetric & Asymmetric Inverter, Power Losses, Semi Cascaded topology, Voltage Drop, Reduction of Circuit Components.

I. INTRODUCTION

Inverters are fundamentally AC to DC converters. The working principle of an inverter is to change DC input voltage to AC output Voltage of desired magnitude and frequency. Ideally the output voltage waveforms of inverters should be sinusoidal however, they are non sinusoidal and contain harmonics. For low and medium power applications, square wave or quasi wave voltages may be competent but for high power application, low distorted sinusoidal waveforms are required. Nowadays with the accessibility of high speed power semiconductor devices, the harmonics contents of output voltage can be minimized or reduced by a huge amount by using different switching techniques[1].

The most attractive features of multilevel inverters are as follows:

1. They can produce output voltages with extremely low distortion and lower dv/dt[3].
2. They draw input current with very low distortion[3].
3. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition,using sophisticated modulation methods, CM voltagescan be eliminated[3].
4. They can operate with a lower switching frequency[3].

These properties make multilevel converters very attractive to the industry and, nowadays, researchers all overthe world are spending great effortstrying to improve multilevel converter performances such as the control simplification and the performance of different optimization algorithms in order to enhance the THD of the output signals, the balancing of the dc capacitor voltage, and the ripple of the currents[2]. These days researchers are focused on the harmonic elimination using recalculated switching functions , harmonic mitigation to fulfill specific grid codes , the developmentof new multilevel converter topologies (hybrid or new ones) , and new control strategies[1].
The most common multilevel inverter configurations are[1]

1. Neutral point clamped (NPC) multilevel inverter
2. Cascaded H-bridge (CHB) multilevel inverter
3. Flying capacitor multilevel (FC) inverter.

The main drawbacks of three topologies are the deviating voltage of neutral point voltage in NPC,unbalance voltage in dc link of FC,large number of separated dc supplies in CHB[1]-[2].

Other topologies are also introduced with time. Lately, hybrid multistage and asymmetrical multilevel inverter topologies are admired in research area. The cost and size of the inverter is reduced and dependability is improved since minimum number of electronic components,capacitors and dc supplies are used in the inverter[3].The hybrid multilevel inverter is a different multilevel inverter configuration with different number of dc supplies.With such converter different modulation

strategies and control systems such as sinusoidal pulse width modulation(SPWM),selective harmonic elimination(SHE-PWM),space vector modulation(SVM) and others are developed.Bidirectional switches with an appropriate control technique can improve the performance of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels[9].

II. THREE PHASE ASYMMETRICAL HYBRID TOPOLOGY

The new topology consists ofthree bidirectional switches (S_1–S_2, D_{a1}–D_{c2}), two switches–two diodes type, are added to the conventional three-phase two-level bridge (Q_1–Q_6). The bidirectional switches are used to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of $4V_{dc}$ and CHB having two unequal dc voltage supplies of V_{dc} and $2V_{dc}$ are connected to (+, –, o) bridge terminals. The CHB cells are used to obtain desired number of output level. Since the new topology inverter is designed to achieve five voltage levels, the power circuit of the CHB makes use of two series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels. The first cell dc voltage supply V_{dc} is added if switch T_1 is turned ON leading to $V_{mg}=+V_{dc}$ where V_{mg} is the voltage at node (m) with respect to inverter ground (g) or bypassed if switch T_2 is turned ON leading to $V_{mg}=0$. Similarly, the second cell dc voltage supply $2V_{dc}$ is added when switch T_3 is turned ON resulting in $V_{om}=+2V_{dc}$ where V_{om} is the voltage at midpoint (o) with respect to node (m) or bypassed when switch T_3 is turned ON resulting in $V_{om}=0$. [2]

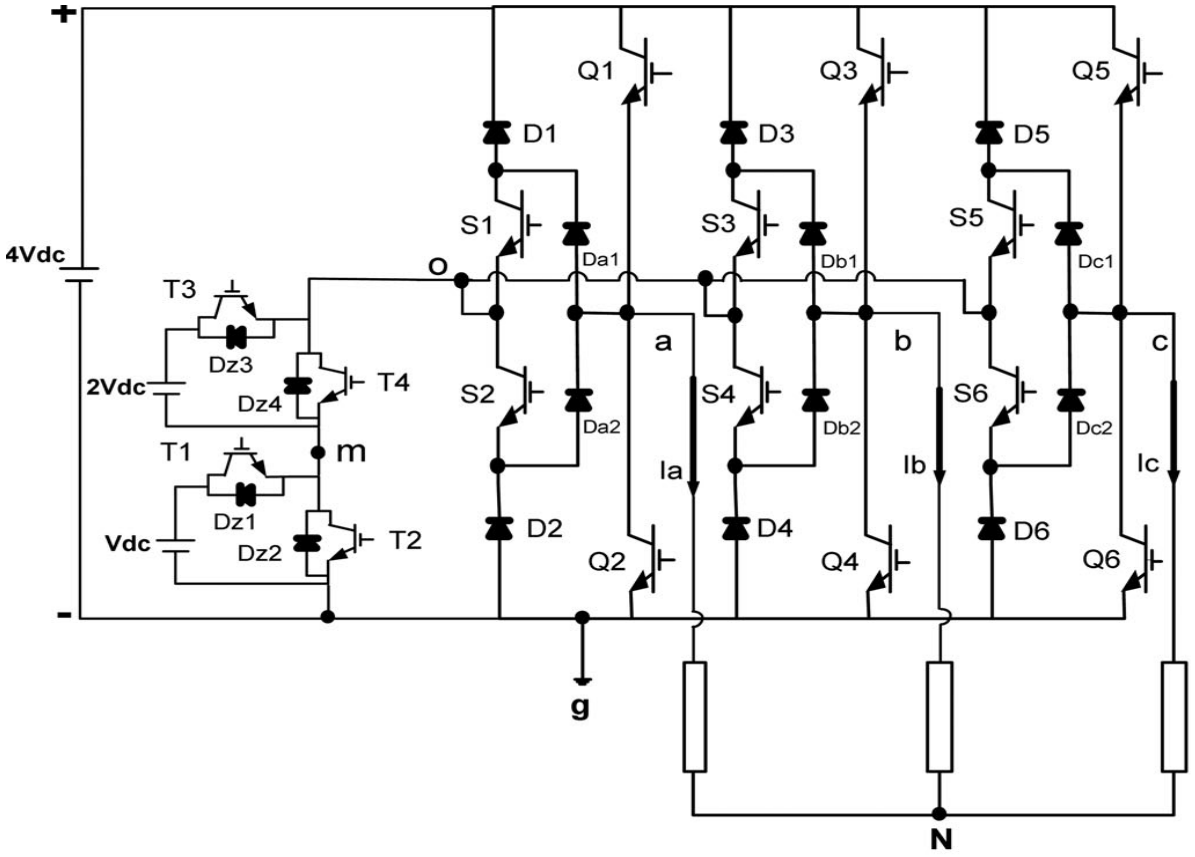


Figure 1 Three phase asymmetrical hybrid topology[2]

As suggested the control strategies of the existing Multilevel inverter is quite complex and time consuming so it is thoughtful process to develop a control strategy which is not complex and time consuming.

- Fundamental frequency considered to be 50 Hz therefore the time period of one cycle is 20 ms.
- Now togenerate five level in output phase voltage means total 5 steps in one cycle, four steps for positive voltage , four steps for negative voltage and one zero level.
- If we trace output voltage it contains total 24 steps in one complete cycle. So 20 ms is of one cycle and 24 steps in output voltage. For simplicity we consider that every step is for 1 ms and then change to another step.
- As we get 24 steps in one cycle but to generate every step with particular level we have to trace the switching position. Means to get 0 level how many switches turn ON and How many switches turn OFF.

Table 1 Switching table

Switches	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4
t_1	1	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1
t_2	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	1
t_3	1	0	0	0	0	1	0	0	1	1	0	0	0	1	1	0
t_4	1	0	0	0	0	1	0	0	1	1	0	0	1	0	1	0
t_5	1	0	1	0	0	1	0	0	0	0	0	0	1	0	1	0
t_6	0	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0
t_7	0	0	1	0	0	1	1	1	0	0	0	0	0	1	1	0
t_8	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	1
t_9	0	1	1	0	0	1	0	0	0	0	0	0	1	0	0	1
t_{10}	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	1
t_{11}	0	1	1	0	0	0	0	0	0	0	1	1	0	1	1	0
t_{12}	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1	0
t_{13}	0	1	1	0	1	0	0	0	0	0	0	0	1	0	1	0
t_{14}	0	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0
t_{15}	0	1	0	0	1	0	0	0	1	1	0	0	0	1	1	0
t_{16}	0	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1
t_{17}	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1
t_{18}	0	0	0	1	1	0	1	1	0	0	0	0	1	0	0	1
t_{19}	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0
t_{20}	0	0	0	1	1	0	1	1	0	0	0	0	1	0	1	0
t_{21}	1	0	0	1	1	0	0	0	0	0	0	0	1	0	1	0
t_{22}	1	0	0	1	0	0	0	0	0	0	1	1	1	0	1	0
t_{23}	1	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0
t_{24}	1	0	0	1	0	0	0	0	0	0	1	1	1	0	0	1

For this we have to make a Vector of every switches by tracing each level than apply it to switches accordingly.

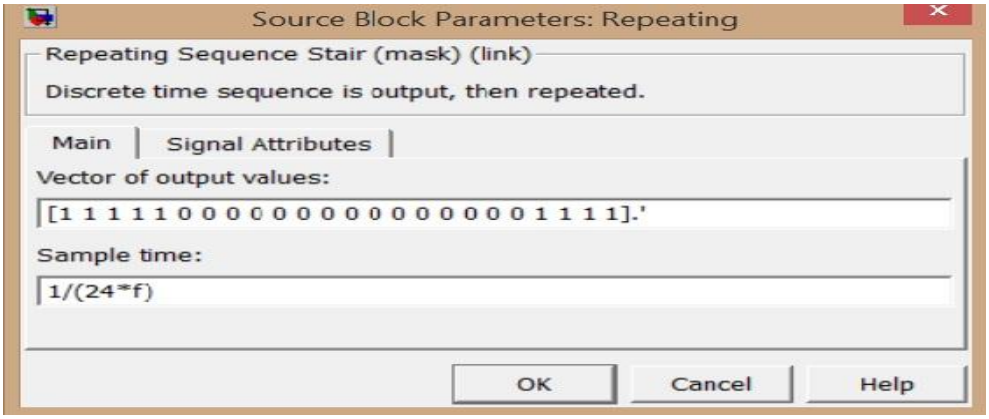


Figure 2 vector of a switch

The above figure shows the repeating sequence of Q1 which is defines in a form of vector in 24 different states.

III. SIMULATION & EXPERIMENTAL RESULTS

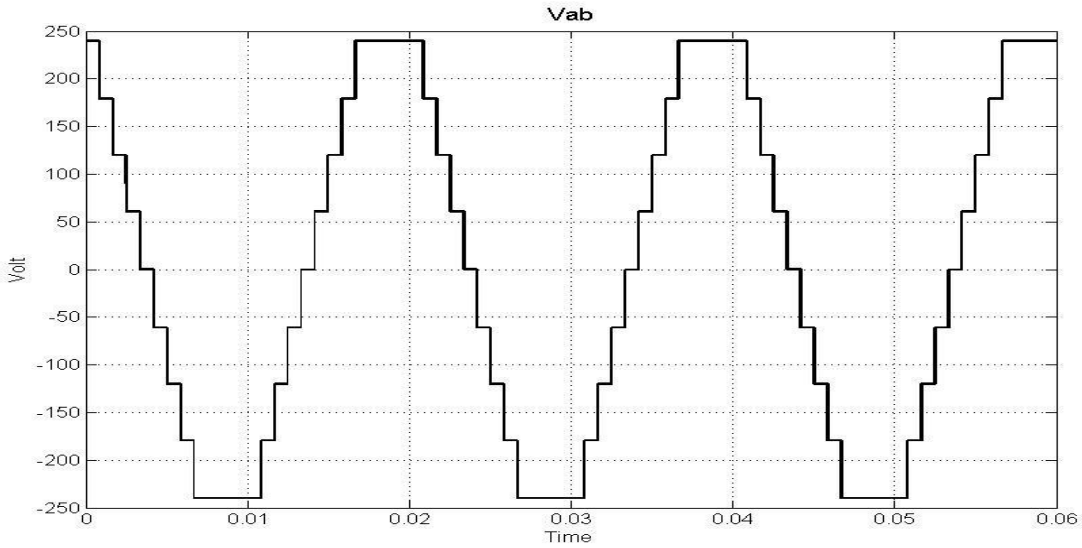


Figure 3 V_{ab}

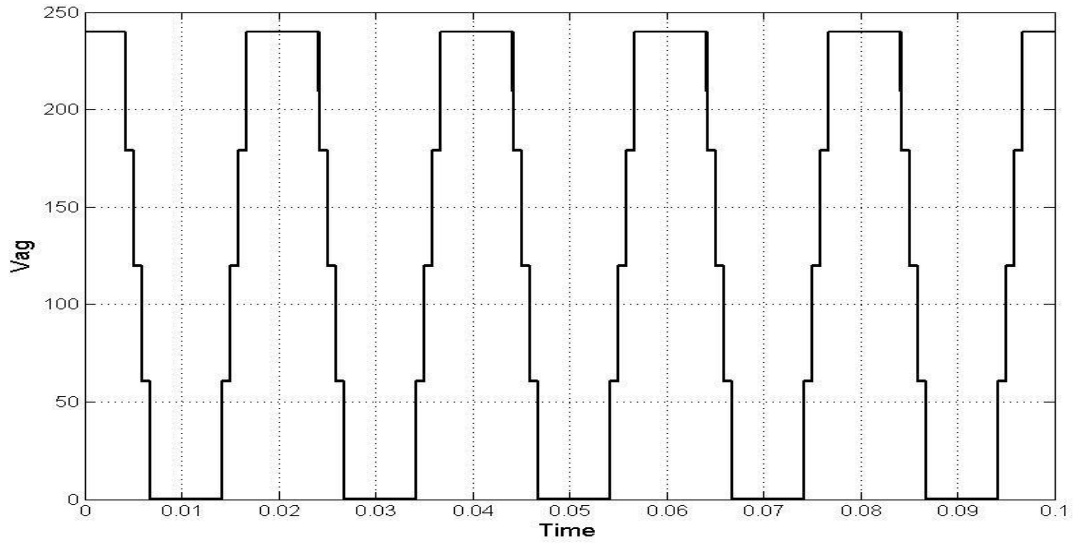
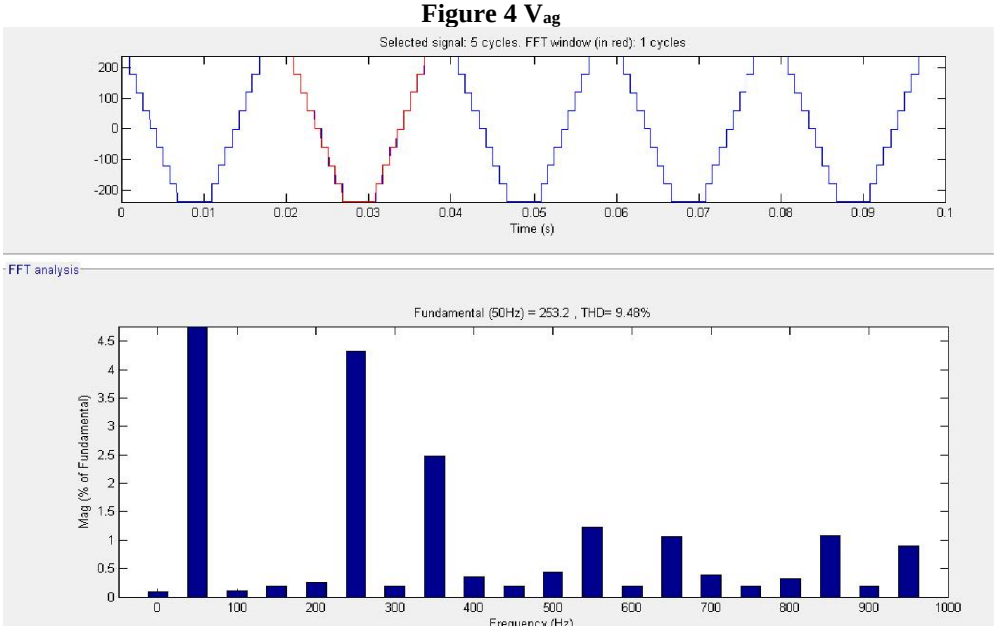


Figure 4 V_{ag}



CONCLUSION

In this paper, a new topology for three phase multilevel inverter which has reduced number of switches is studied. The new asymmetrical hybrid topology requires smaller amount of dc sources and gate driver circuits. To implement the inverter circuit, lower number of required devices results in to reduction in cost of the inverter and makes the control scheme comparatively simple. A prototype of three phase asymmetrical hybrid multilevel inverter is simulated for 5 levels. Harmonic distortion of the given topology is around 9.48%.

ACKNOWLEDGMENT

First and foremost, all gratitude to the omnipresent god for giving me the strength through my prayers and to plod me on despite the difficult situations I passed through till my graduation. I would like to express my gratitude towards my supervisor Prof. Ami Vyas , for her cooperation, guidance, inspiration, and valuable advices while doing this project. In addition, i sincerely thank all the lecturers who have taught me, for the lessons that have been delivered and the morals the have been gained. Not to forget mentioning my fellow friends, I would like to thank them for sharing useful ideas, information and moral support during the course of study. Last but not least, I would like to express my love, gratitude and appreciation to my beloved parents and brothers for their love, patience, support and encouragement they provide during my study.

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